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10/593,695	09/20/2006	Yasuhiko Nakashima	1035-660	4019

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EXAMINER	
ALROBAYE, IDRISS N	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,695	NAKASHIMA, YASUHIKO	
	Examiner	Art Unit	
	IDRISS N. ALROBAYE	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *18-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8-11,13 and 15-17* is/are rejected.

7)☐ Claim(s) *5-7,12 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/09/2009, 4/06/2009, 9/20/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is responsive to supplemental response received on 12/04/2009.

2. Claims 1-17 are presented for examination.

3. Claims 18-29 are withdrawn.

4. Claims 30-31 are cancelled.

5. Applicant's amendments to the specification have been considered and the specification objections have been withdrawn.

6. Applicant's amendments to claims 16-17 and cancellation of claims 30-31 have been considered and the claim objections have been withdrawn.

7. The IDS filed 9/20/2006 have been considered according to the explanation of the remarks filed on 7/15/2009, page 20. The IDS objections have been withdrawn.

8. Applicant's cancellation of claim 30 has been noted and the 35 USC 101 rejections have been withdrawn.

9. Applicant's amendments and arguments to the claims to overcome 35 USC 112 1st and 2nd paragraph have been considered and the rejections have been withdrawn.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-4, 8-11, 13, 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miki U.S. Patent No. 6,810,474 in view of Huang U.S. Patent No. 4,943,909.

12. As per claim 1, Miki teaches a data processing device which reads out program instructions from an instruction region in a main memory and writes a result of a computation into the main memory (see Fig. 1 and col. 4, lines 8-41),

the data processing device comprising:

first computing means for performing a computation based on one or more instructions in the instruction region which are read out from the main memory (see Fig. 1, and col. 4, lines 35-40);

a register by which the first computing means writes data and reads to/from the main memory (Fig. 1, element 118);

input/output group generating means for generating an input/output group, which is made up of an input pattern comprising one or more elements and an associated output pattern comprising one or more output elements at the time of execution of one or more program instructions in the instruction region by the first computing means (Fig. 3, and col. 8, lines 43-67); and

input/output group storage means for storing the input/output group in an instruction region storage section of the input/output group generating means (col. 8, line 43 to col. 9, line 8), wherein

at the time of execution of instructions read out from the instruction region in main memory, if an input pattern in the instruction region is matched with an input pattern in the input/output group, the first computing means performs a reuse operation that outputs the associated output pattern to the register and/or the main memory, (Fig. 3 and col. 8, line 43 to col. 9, line 8; see also col. 9, line 62 to col. 10, line 26), and wherein

Miki shows dependency relations storage (see col. 2, line 8-44) but did not specifically go into the details of input element and output element derives. However, Huang teaches indication from which input element in the input pattern each output element in the output pattern derives; and input/output group setting means for setting, based on stored dependency relations information, an input/output group that is made up of an output pattern including at least one said output element and an input pattern including at least one said input element (see Huang, Fig. 3 and col. 5, lines 16-51), for the purpose of realization of any computing function with a regular array of interconnected processing elements.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Huang in invention of Miki, for the purpose of realization of any function within a regular array of interconnected elements thus allowing highly parallel computations which significantly improves performances.

13. As per claim 2, Miki in view of Huang further teaches the data processing device as defined in claim 1, wherein,

if a first group of input elements from which a first output element is derived, is included entirely within a second group of input elements from which a second output element different from the first output element is derived, the input/output group setting means sets (i) the second group as the input pattern and (ii) the first group and the second group as the output pattern (see Huang, col. 5, lines 16-67 and see also Miki col. 8, lines 43-67).

14. As per claim 3, Miki in view of Huang further teaches the data processing device as defined in claim 1, wherein,

If there is no shared input element between a first group of input elements from which a first output element is derived, and a second group of input elements from which a second output element different from the first output element is dervied, the input/output pattern group setting means sets (i) a first input/output group in which the first group of the input elements is the input pattern and the first output element is the output pattern and (ii) a second input/output group in which the second group of the input elements is the input pattern and the second output element is the output pattern (see Huang, col. 5, lines 16-67 and see also Miki col. 8, lines 43-67).

15. As per claim 4, Huang further teaches the data processing device as defined in claim 1, wherein

the dependency relations storage section is made up of a two-dimensional (2D) matrix-arranged memory portion in which row elements of the matrix-arranged memory are stored with the output elements and column elements of the matrixed-arranged memory are stored with the input elements, and each memory of the 2D matrix-arranged memory includes information indicating whether or not an output element corresponding to a row element is derived from an input element corresponding to a column element (see Huang, Fig. 3 and col. 5, lines 16-67).

16. As per claim 8, Huang further teaches the data processing device as defined in any claim 1, further comprising at least one second computing means,

wherein in regard of the instruction region processed by the first computing means, the second computing means subjects the instruction region to a computation based on a predicted input value, and registered a result of the computation in the instruction region storage means (col. 5, lines 16-51).

17. As per claim 9, Miki further teaches the data processing device as defined in claim 1, wherein,

the input/output group setting means further comprises: an output-side group storage section which stores information of an input/output group to which each of the output elements belongs; an input-side group storage section which stores information of an input/output group to which each of the input elements belongs; a temporal storage section which stores a changed dependency relation between an output

element and an input element, whenever there is a change in information stored in the dependency relations storage section while the input/output group is generated; and a group temporal storage section which stores information of a changed input/output group when there is a change in information stored in the dependency relations storage section while the input/output group is generated (Fig. 3, and col. 8, lines 43-67 and col. 4, lines 35-40).

18. As per claim 10, Miki further teaches the data processing device as defined in claim 9, wherein

the input/output group setting means further includes a group management section that stores information of the input/output group which has previously been allocated to the output element and/or the input element while the input/output group is generated (Fig. 3, and col. 8, lines 43-67 and col. 8, line 43 to col. 9, line 8),

19. As per claim 11, Huang further teaches the data processing device as defined in claim 9, wherein

the dependency relations storage section is made up of a two-dimensional (2D) matrix-arranged memory portion in which row elements of the matrix-arranged memory are stored with the output elements and column elements of the matrix-arranged memory are stored with the input elements, and each memory element of the 2D matrix-arranged memory includes information indicating whether or not an output element

corresponding to a row element is derived from an input element corresponding to a column element (see Huang, Fig. 3 and col. 5, lines 16-67).

20. As per claim 13, Miki further teaches the data processing device as defined in claim 9, wherein

the input/output group setting means further includes a conditional branch storage section that stores information regarding an input element on which the conditional branch instruction depends whenever a conditional branch instruction is detected while the input/output group is generated (see col. 4, lines 8-41).

21. As per claim 15, Miki further teaches the data processing device as defined in claim 1, wherein, the instruction region storage section includes input pattern storage section which stores input patterns as a tree structure in which items that are to be subjected to equal comparison are regarded as nodes (Fig. 3, and col. 8, lines 43-67).

22. As per claim 16, Miki further teaches the data processing device as defined in claim 15,

further comprising input pattern storage means that organizes the tree structure in such a manner that a value of an item in the input pattern, which item is subjected to equal comparison, is stored in association with an item which is to be next subjected to a comparison (see col. 8, lines 15-67).

23. As per claim 17, Huang further teaches the data processing device as defined in claim 16, wherein, the input pattern storage means further includes an associative search means and an additional information storage section, wherein the associative search means includes one or more search target lines that include a value storage area in which a value of an item to be subjected to equal comparison is stored, and a key storage area where a key for identifying each item is stored; and the additional information storage section a search item designation area in which an item to be next subjected to associative search is stored in accordance with a line corresponding to said one or more search target line (col. 10, lines 24-60 and col. 8, lines 1-59).

Allowable Subject Matter

24. Claims 5-7, 12 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

25. Applicant's arguments filed 7/15/2009 have been fully considered but they are not persuasive.

Applicant's argument:

"In a brief discussion of background prior art, Miki makes some references to the use a memory for storing the past execution results of an instruction which may be later output and used depending to some extent on whether or not consecutive or subsequent instructions have some degree of data dependency. However, the memory

disclosed the memory disclosed and discussed by Miki is not a "dependency relations information storage" as recited in Applicant's claims. In contrast to Miki's memory, Applicant's dependency relations information storage is a memory that is used to store "dependency relations" information regarding I/O data patterns for groups of instructions rather than for the storage only of past execution results. For at least this reason, Applicant respectfully contends that Miki does not teach and does not in the least bit suggest the use of such a "dependency relations storage" as set forth in Applicant's claims. Moreover, as the Office Action admits, Miki does not describe any details of how Applicant's claimed input and output elements are derived. (Office Action at page 11, para. 2.)"

Examiner's response:

The examiner respectfully disagrees because the applicant did not explicitly define the 'dependency relations information storage'. However, it's understood to be a storage that stores dependency information which was explicitly shown in Mike, col. 2, lines 8-44. Mike's memory stores data that results from instruction dependency which reads on applicant's dependency relations information storage. However, Mike did not describe the detail of input/output elements. However, the secondary reference Huang teaches indication which input element in the input pattern each output element in the output pattern derives; and input/output group setting means for setting, based on stored dependency relations information, an input/output group that is made up of an output pattern including at least one said output element and an input pattern including at least one said input element (see Huang, Fig. 3 and col. 5, lines 16-51).

Applicant's argument:

"However, as evident from Figure 3, this particular passage in Huang discloses only that a right input of each Processing Element (PE) in an array is physically connected to (i.e., "derived") from the left output of a PE from a preceding row in the same column, and that the left input of each PE is obtained from the right output of a PE of a preceding row in the left adjacent column. The disclosed explanations by Huang of

physical interconnections of multiple Processing Elements has no relationship to the deriving or storing of dependency relationship information between input and output patterns of executed instructions groups in the manner as set forth in Applicant's independent claims. Consequently, for the sake of argument only, even if the teachings of Huang could be combined with the teachings of Miki, the result would certainly not be operable in the manner as set forth in Applicant's claims.

The Office Action fails to cite prior art that remedies the deficiencies of Miki as set forth above, or to suggest any motivation to modify Miki to arrive at the claimed invention. There is no objective teaching or disclosure anywhere in Huang of modifying the Miki system to provide a means for generating an I/O group which includes a dependency relations storage section or a means for generating dependency relations information that indicates which input element in an input pattern in an I/O group that each output element in an associated output pattern is derived, as set forth in Applicant's claims. Likewise, the Office Action has failed to provide any objective basis that would have motivated one of skill in the art to modify Miki's system to provide Applicant's claimed data processing device."

Examiner's response:

The examiner respectfully disagrees. With respect to the dependency relation information storage, Miki shows a memory that stores result of instruction dependency but Miki's did not show the detail on the input/output elements pattern. However, Huang shows input/element pattern with respect to the dependency relation information, thus combining both reference reads on applicant's claim language. Furthermore, the examiner would like to remind the applicant's that a rejection is based on the broadest reasonable interpretation of the claim language along with explicit and unambiguous definitions for the claim language which must be made available in the specification. The instant application did not provide any explicit definitions for the argued elements of claim 1, including the dependency relation information storage.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by

combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one having an ordinary skill in the relevant art to combine the teachings of Huang in the invention of Miki, for purpose of realization of any function within a normal array of interconnected elements, thus allowing highly parallel computations which significantly improves performances and reduces latency.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDRISS N. ALROBAYE whose telephone number is (571)270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
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